

74 are added to recite subject matter to which Applicant is already entitled. Applicant submits that no issue of new matter has been set forth by this Amendment. Accordingly, claims 1-6, 9-10, 15-16, 22-27, 40 and 46-74 are now pending in the subject application and are believed to be in condition for allowance at least for the reasons advanced hereinbelow.

Initially, the Office Action appears to object to the Title of Invention as non-descriptive. By the above Amendment, the Title of Invention has been replaced with one which is indicative of the invention to which the claims are directed. In particular, the new Title of Invention recites --SEMICONDUCTOR DEVICE--.

The Office Action rejects claim 1 under 35 U.S.C. §102(e) as anticipated by *Sato et al.* (U.S. Patent No. 6,081,305), claims 2 and 13-14 under 35 U.S.C. 103(a) as unpatentable over *Sato et al.* in view of *Yamazaki* (U.S. Patent No. 5,990,542), claim 3 under 35 U.S.C. 103(a) as unpatentable over *Sato et al.* in view of *Okita* (U.S. Patent No. 6,097,453), claim 4 under 35 U.S.C. 103(a) as unpatentable over *Sato et al.* in view of *Okita* and *Yamazaki*, claims 5, 7-8, 13-14, 16, 22-27, 40 and 46 under 35 U.S.C. 103(a) as unpatentable over *Sato et al.* in view of *Fukunaga* (U.S. Patent No. 5,706,064), claims 6 and 15 under 35 U.S.C. 103(a) as unpatentable over *Sato et al.* in view of *Jun* (U.S. Patent No. 5,948,705), and claims 9-10 under 35 U.S.C. 103(a) as unpatentable over *Jun* in view of *Fukunaga*. By the above Amendment, claims 7-8 and 13-14 are canceled without prejudice, thereby rendering any rejection moot with respect thereto. Claims 1-4, 16, 22-27 and 40 have been amended in order to more clearly define subject matter which Applicant is already entitled. This fact notwithstanding, Applicant traverses the grounds for rejection at least for the reasons set forth hereinbelow.

As presently recited at least in claims 1-6, the claimed invention is directed generally to a semiconductor device comprising at least one transistor (i.e., a first conductive layer), at least one interlayer insulating film formed over said transistor, said interlayer insulating film having at least one contact hole, an embedded conductive layer provided to fill said contact

hole, wherein a top surface of said embedded conductive layer is flush with a top surface of said interlayer insulating film, and a reflective pixel electrode (i.e., a second conductive layer) formed on said interlayer insulating film, wherein the embedded conductive layer comprises a conductive material dispersed in a medium, the conductive material being selected from the group consisting of carbon, zinc oxide, aluminum, and nickel. Such a design is advantageous since it allows an etch back or CMP (Chemical Mechanical Polishing) to be performed in order to provide a leveled upper surface over the contact hole. As a result, the pixel electrode formed on the embedded conductive layer can maintain complete flatness at an upper surface thereof (i.e., a leveled upper surface).

As the Examiner well knows, "a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. Of California*, 814 F.2d 628, 631, 2 USPQ2d 1051 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the...claims." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913 (Fed. Cir. 1989).

Moreover, a four-level factual inquiry must be taken when formulating a rejection under 35 USC §103. First, a determination of the scope and content of the prior art. Second, an ascertainment of the differences between the claimed invention and the prior art. Third, a resolution of the level of ordinary skill in the pertinent art. Fourth, an evaluation of objective evidence of non-obviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). In essence, to establish a *prima facie* case of obviousness, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 180 USPQ 580 (CCPA 1974).

Applicant respectfully contends that the claims as presently recited set forth subject matter which is clearly patentably distinct over the prior art of record. More particularly, Applicant respectfully contends that the *Sato et al.* patent, either alone or in combination with the *Yamazaki*, *Okita*, *Jun* and *Fukunaga* patents, fails to expressly teach or inherently

suggest all of the limitations presently set forth in the claimed invention necessary to support a finding of anticipation under §102 or obviousness under §103.

Referring now to the Office Action, which finds that the *Sato et al.* patent teaches a semiconductor device including wiring 141 (with regards to the first conductive layer 101 in Fig. 1) connected to the pixel electrode 181 (regards to the second conductive layer 105 in Fig. 1) via a through hole 171 (regards to the embedded layer 104 in Fig. 1) as shown in Fig. 2, column 15, lines 2-4.

However, the claimed invention teaches that the embedded conductive layer and the second conductive layer are individually formed. The *Sato et al.* patent fails to expressly teach or inherently suggests the separate formation of an embedded conductive layer provided to fill the contact hole and a second conductive layer provided for placement on the contact hole. Moreover, the *Sato et al.* patent fails to expressly teach or inherently suggests a semiconductor device having an embedded conductive layer comprising a conductive material selected from the group consisting of carbon, zinc oxide, aluminum, and nickel, as presently set forth in the claimed invention.

Moreover, Applicant contends that there is a lack of motivation in the cited references to achieve the claimed invention. Note that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion or motivation to do so found in the references themselves or in the knowledge generally available to one of ordinary skill in the art. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

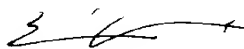
In the subject application, claim 6 is directed generally to a semiconductor device comprising a conductive layer and a reflective pixel electrode formed on said conductive layer, wherein at least one peripheral edge of said reflective pixel electrode is coextensive with a peripheral edge of said conductive layer. The Office Action finds that the *Yamazaki* patent fails to disclose a metal electrode formed on the conductive layer as claimed, and

thus, provides the *Jun* patent to modify the teachings of *Yamazaki* since *Jun* allegedly teaches the above-noted metal electrode in a Fig. 4 illustration. The *Jun* patent, however, fails to expressly teach or implicitly disclose a conductive material pattern provided for the formation of a pixel electrode. Accordingly, there is a lack of motivation or suggestion in either of the cited references or in the knowledge generally available to a skilled artisan to modify the teaching of *Yamazaki* in order to achieve the claimed invention.

Accordingly, since the *Sato et al.* patent, either alone or in combination with the *Yamazaki*, *Okita*, *Jun* and *Fukunaga* patents, fails to expressly teach or inherently suggests each and every feature of the claimed invention necessary to support a finding of anticipation under §102 or obviousness under §103, and also lacks motivation or suggestion to modify the their respective teachings in order to achieve the claimed invention, reconsideration and withdrawal of the rejection is respectfully solicited.

Accordingly, Applicant respectively submits that the pending claims are in proper condition for allowance and consideration and withdrawal of the pending rejections are requested. If the Examiner believes further discussions with Applicant's representative would be beneficial in this case, he is invited to contact the undersigned.

Respectfully submitted,



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## MARKED UP VERSION OF AMENDED CLAIMS

1. (Twice Amended) A semiconductor device comprising:

at least one transistor;

at least one interlayer insulating film formed over said transistor, said interlayer insulating film having at least one contact hole;

an embedded conductive layer provided to fill said contact hole, wherein a top surface of said embedded conductive layer is flush with a top surface of said interlayer insulating film; and

a reflective pixel electrode formed on said interlayer insulating film, wherein said reflective pixel electrode is electrically connected to said transistor through said embedded conductive layer,

wherein the embedded conductive layer comprises a conductive material dispersed in a medium, the conductive material being selected from the group consisting of carbon, zinc oxide, aluminum, and nickel.

2. (Twice Amended) A semiconductor device comprising:

at least one transistor;

at least one interlayer insulating film comprising an organic resin formed over said transistor, said interlayer insulating film having at least one contact hole;

an embedded conductive layer provided to fill said contact hole, wherein a top surface of said embedded conductive layer is flush with a top surface of said interlayer insulating film; and

a reflective pixel electrode formed on said interlayer insulating film, wherein said reflective pixel electrode is electrically connected to said transistor through said embedded conductive layer,

wherein said embedded conductive layer comprises a conductive material dispersed in a medium, said conductive material being selected from the group consisting of carbon, zinc oxide, aluminum, and nickel.

3. (Twice Amended) A semiconductor device comprising:

at least one transistor;

a first interlayer insulating film formed over said transistor;

a drain electrode formed on said first interlayer insulating film and electrically connected to a drain of said transistor through an opening of said first interlayer insulating film;

a second interlayer insulating film formed over said drain electrode and said first interlayer insulating film;

a capacitor forming electrode formed on said second interlayer insulating film to form a capacitor between said drain electrode and said capacitor forming electrode;

a third interlayer insulating film formed over said capacitor forming electrode and said second interlayer insulating film;

a contact hole opened through said third and second interlayer insulating films to reach said drain electrode;

an embedded conductive layer filled in said contact hole; and

a reflective pixel electrode formed on said third interlayer insulating film, wherein said reflective pixel electrode is electrically connected to said drain electrode through said embedded conductive layer,

wherein said embedded conductive layer comprises a conductive material dispersed in a medium, said conductive material being selected from the group consisting of carbon, zinc oxide, aluminum, and nickel.

4. (Twice Amended) A semiconductor device comprising:  
at least one transistor;  
a first interlayer insulating film formed over said transistor;  
a drain electrode formed on said first interlayer insulating film and electrically connected to a drain of said transistor through an opening of said first interlayer insulating film;  
a second interlayer insulating film formed over said drain electrode and said first interlayer insulating film;  
a capacitor forming electrode formed on said second interlayer insulating film to form a capacitor between said drain electrode and said capacitor forming electrode;  
a third interlayer insulating film comprising an organic resin formed over said capacitor forming electrode and said second interlayer insulating film;  
a contact hole opened through said third and second interlayer insulating films to reach said drain electrode;  
an embedded conductive layer filled in said contact hole; and  
a reflective pixel electrode formed on said third interlayer insulating film, wherein said reflective pixel electrode is electrically connected to said drain electrode through said embedded conductive layer,  
wherein said embedded conductive layer comprises a conductive material dispersed in a medium, said conductive material being selected from the group consisting of carbon, zinc oxide, aluminum, and nickel.

16. (Twice Amended) A semiconductor device according to any one of claims [1 to 6] 1-6 or 47-50, further comprising an alignment film.

22. (Twice Amended) A semiconductor device according to [claim 1, 2, 3, 4, 5, or 6,] claims 1-6 or 47-50 wherein said device is a display device of a cellular phone.

23. (Twice Amended) A semiconductor device according to [claim 1, 2, 3, 4, 5, or 6,] claims 1-6 or 47-50 wherein said device is a display device of a camcorder.

24. (Twice Amended) A semiconductor device according to [claim 1, 2, 3, 4, 5, or 6,] claims 1-6 or 47-50 wherein said device is a display device of a portable computer.

25. (Twice Amended) A semiconductor device according to [claim 1, 2, 3, 4, 5, or 6,] claims 1-6 or 47-50 wherein said device is a display device of a head mounting display.

26. (Twice Amended) A semiconductor device according to [claim 1, 2, 3, 4, 5, or 6,] claims 1-6 or 47-50 wherein said device is a display device of a rear type projector.

27. (Twice Amended) A semiconductor device according to [claim 1, 2, 3, 4, 5, or 6,] claims 1-6 or 47-50 wherein said device is a display device of a front type projector.

40. (Twice Amended) A semiconductor device according to any one of [claim 1, 2, 3, 4, 5, or 6,] claims 1-6 or 47-50 wherein said device is an EL display device.